FAMILIARISATION OF BASYS 3 ARTIX-7 FPGA BOARD

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks. Although one-time programmable (OTP) FPGAs are available, the dominant types are SRAM based which can be reprogrammed as the design evolves. ASIC and FPGAs have different value propositions, and they must be carefully evaluated before choosing any one over the other. Information abounds that compares the two technologies. While FPGAs used to be selected for lower speed/complexity/volume designs in the past, today's FPGAs easily push the 500 MHz performance barrier. With unprecedented logic density increases and a host of other features, such as embedded processors, DSP blocks, clocking, and high-speed serial at ever lower price points, FPGAs are a compelling proposition for almost any type of design. Due to their programmable nature, FPGAs are an ideal fit for many different markets. As the industry leader, Xilinx provides comprehensive solutions consisting of FPGA devices, advanced software, and configurable, ready-to-use IP cores for markets.

BASYS3 ATRIX-7 FPGA

The Basys 3 board is a complete, ready-to-use digital circuit development platform based on the latest Artix-7™ Field Programmable Gate Array (FPGA) from Xilinx. With its high-capacity FPGA (Xilinx part number XC7A35T-1CPG236C), low overall cost, and collection of USB, VGA, and other ports, the Basys3 can host designs ranging from introductory combinational circuits to complex sequential circuits like embedded processors and controllers. It includes enough switches, LEDs and other I/O devices to allow a large number designs to be completed without the need for any additional hardware, and enough uncommitted FPGA I/O pins to allow designs to be expanded using Digilent Pmods or other custom boards and circuits.

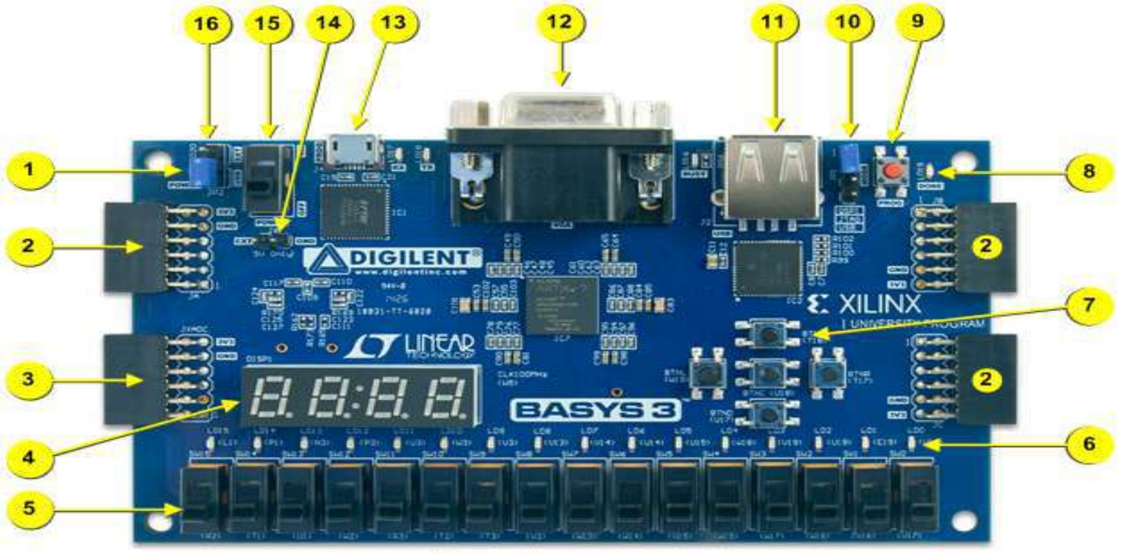
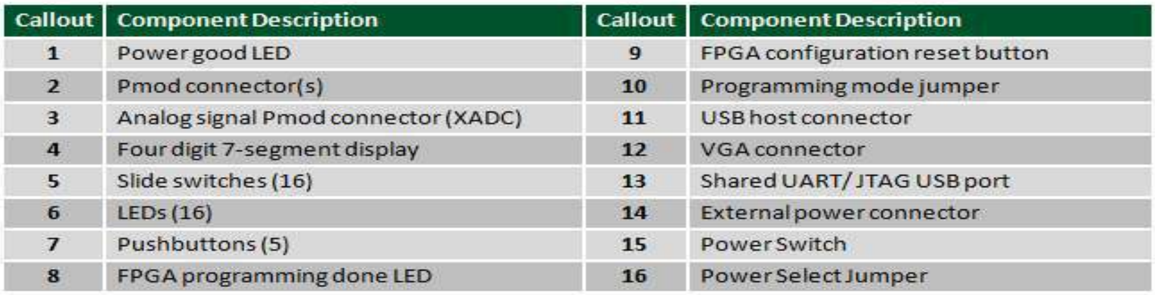


Figure 1. Basys3 board features



Callout	Component Description	Callout	Component Description
1	Power good LED	9	FPGA configuration reset button
2	Pmod connector(s)	10	Programming mode jumper
3	Analog signal Pmod connector (XADC)	11	USB host connector
4	Four digit 7-segment display	12	VGA connector
5	Slide switches (16)	13	Shared UART/ JTAG USB port
6	LEDs (16)	14	External power connector
7	Pushbuttons (5)	15	Power Switch
8	FPGA programming done LED	16	Power Select Jumper

Artix-7 FPGA is optimized for high performance logic, and offers more capacity, higher performance, and more resources than earlier designs. Artix-7 35T features include:

- 33,280 logic cells in 5200 slices
- 1,800 Kbits of fast block RAM
- Five clock management tiles, each with a phase-locked loop (PLL)
- 90 DSP slices
- Internal clock speeds exceeding 450MHz
- On-chip analog-to-digital converter (XADC).

The Basys3 also offers an improved collection of ports and peripherals, including:

- 16 user switches
- 16 user LEDs
- 5 user pushbuttons
- 4-digit 7-segment display
- Three Pmod ports
- Pmod for XADC signals
- 12-bit VGA output
- USB-UART Bridge
- Serial Flash
- Digilent USB-JTAG port for FPGA programming and communication
- USB HID Host for mice, keyboards and memory sticks

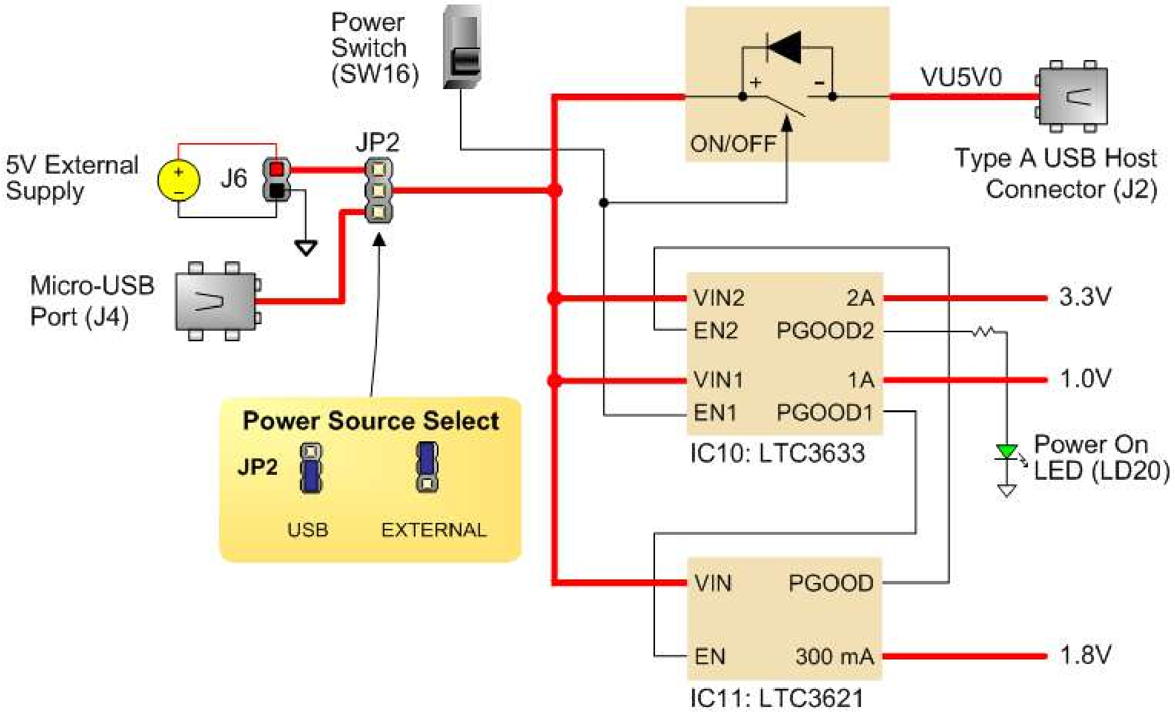
Software--The first Vivado Design Suite Exclusive:

The Basys 3 works with Xilinx's new high-performance Vivado ® Design Suite. Vivado includes many new tools and design flows that facilitate and enhance the latest design methods. It runs faster, allows better use of FPGA resources, and allows designers to focus their time evaluating design alternatives. The System Edition includes an on-chip logic analyzer, high-level synthesis tool, and other cutting-edge tools, and the free "WebPACK" version allows Basys 3 designs to be created at no additional cost.

Power

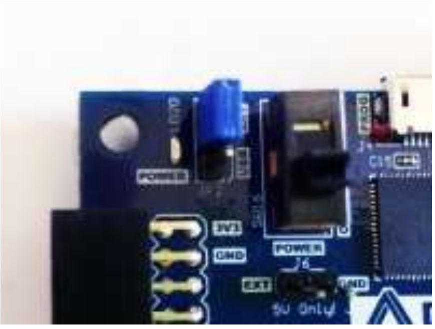
All Basys3 power supplies can be turned on and off by a single logic-level power switch (SW16). A power-good LED (LD20), driven by the "power good" output of the Linear Technologies
LTC3633 http://www.linear.com/product/LTC3633 supply, indicates that the

supplies are turned on and operating normally. An overview of the Basys3 power circuit is shown below.

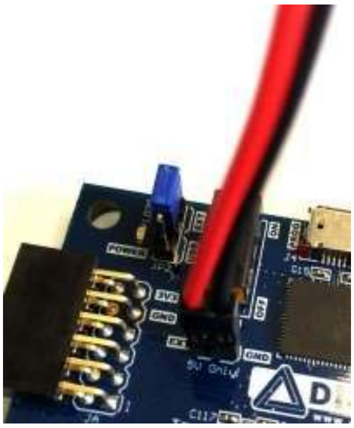


The Basys3 board can receive power from the Digilent USB-JTAG port (J4) or from a 5 volt external power supply (not included). Jumper JP2 (near the power switch) determines which source is used.

USB Power is selected. The USB port can deliver enough power for the vast majority of designs. A few demanding applications, including any that drive multiple peripheral boards, might require more power than the USB port can provide. Also, some applications may need to run without being connected to a PC’s USB port. In these instance an external power supply or battery pack can be used.



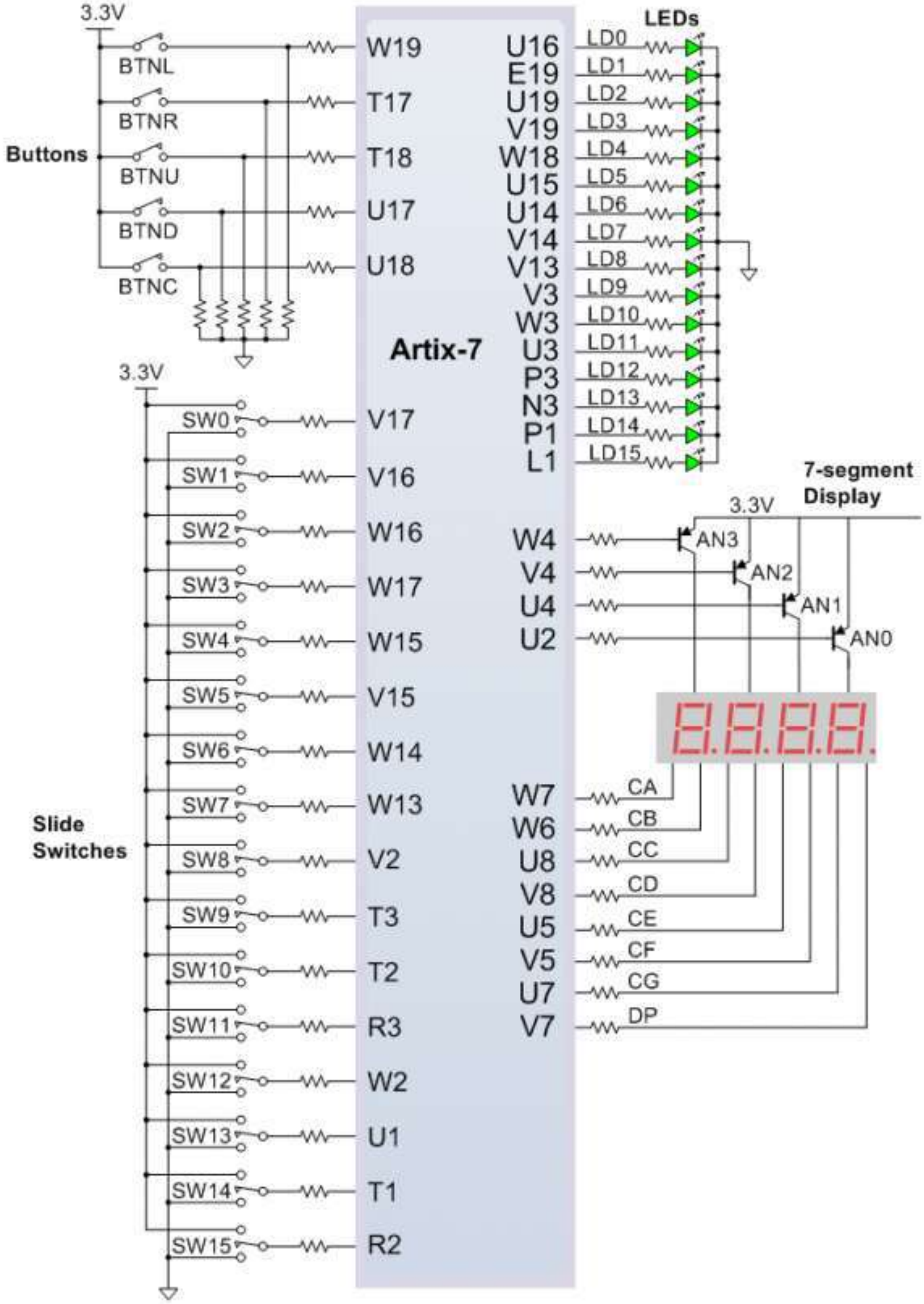
External Power is selected. An external power supply can be used by plugging into the external power header (J6) and setting jumper JP2 to “EXT”. The supply must deliver 4.5VDC to 5.5VDC and at least 1A of current (i.e., at least 5W of power). Many suitable supplies can be purchased through Digikey or other catalog vendors. An external battery pack can be used by connecting the battery’s positive terminal to the “EXT” pin of J6 and the negative terminal to the “GND” pin of J6.



The power provided to USB devices that are connected to Host connector J2 is not regulated. Therefore it is necessary to limit the maximum voltage of an external battery pack to 5.5V DC. The minimum voltage of the battery pack depends on the application -if the USB Host function (J2) is used, at least 4.6V needs to be provided. In other cases the minimum voltage is 3.6V.

Basic I/O

The Basys3 board includes sixteen slide switches, five push buttons, sixteen individual LEDs, and a four-digit seven-segment display, as shown in the below diagram. The pushbuttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output). The five pushbuttons, arranged in a plus-sign configuration, are “momentary” switches that normally generate a low output when they are at rest, and a high output only when they are pressed. Slide switches generate constant high or low inputs depending on their position.

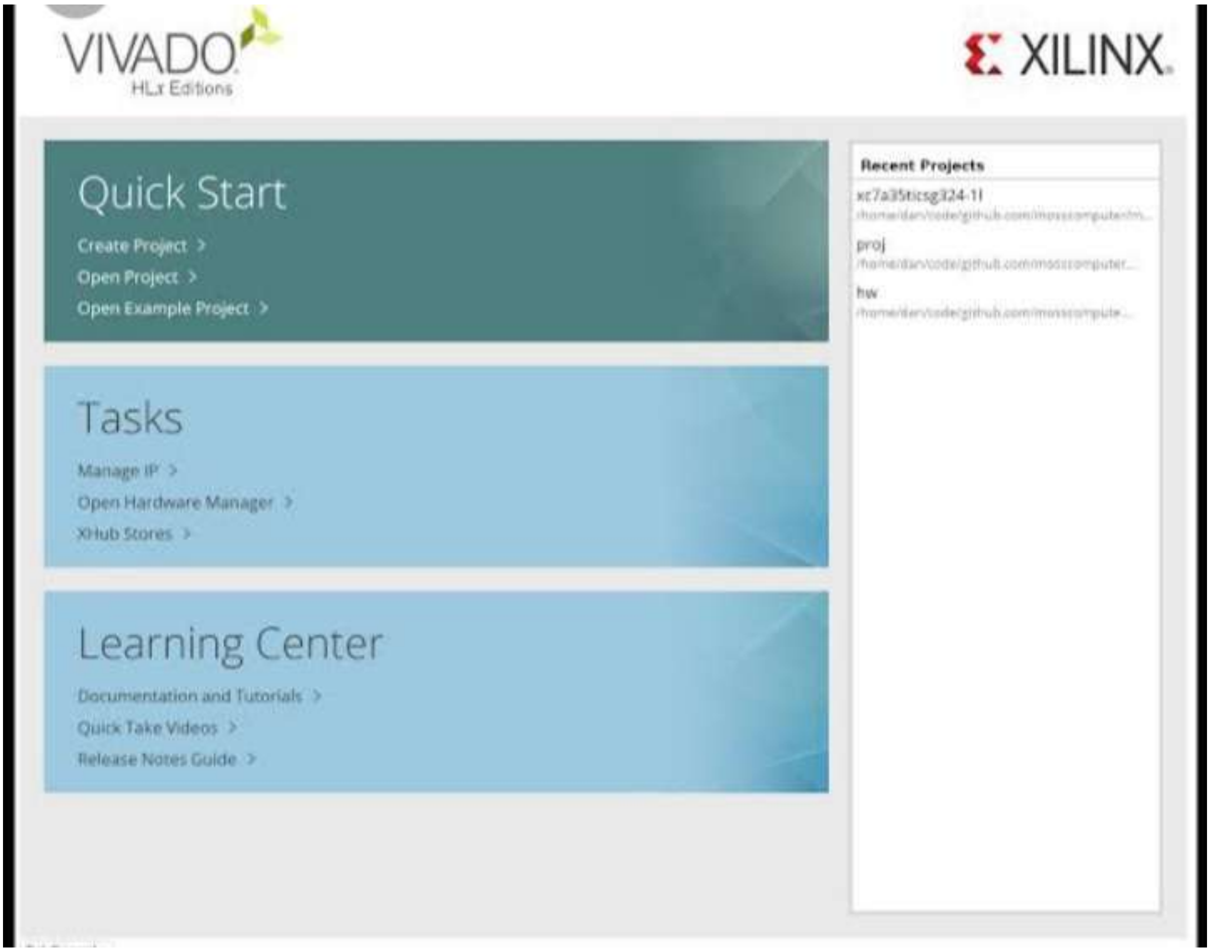

3.3V
Buttons
BTNL
BTNR
BTNU
BTND
BTNC
W19
T17
T18
U17
U18
Artix-7
3.3V
Slide Switches
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
SW15
V17
V16
W16
W17
W15
V15
W14
W13
V2
T3
T2
R3
W2
U1
T1
R2
LEDs
U16
E19
U19
V19
W18
U15
U14
V14
V13
V3
W3
U3
P3
N3
P1
L1
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LD8
LD9
LD10
LD11
LD12
LD13
LD14
LD15
7-segment Display
3.3V
W4
V4
U4
U2
AN3
AN2
AN1
AN0
W7
W6
U8
V8
U5
V5
U7
V7
CA
CB
CC
CD
CE
CF
CG
DP

VIVADO

Vivado Design Suite is a software suite produced by Xilinx for synthesis and analysis of HDL designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis. Vivado represents a ground-up rewrite and re-thinking of the entire design flow (compared to ISE). Like the later versions of ISE, Vivado includes the in-built logic simulator ISIM.Vivado also introduces high-level synthesis, with a toolchain that converts C code into programmable logic. Replacing the 15 year old ISE with Vivado Design Suite took 1000 person-years and cost US$200 million

Components

The Vivado High-Level Synthesis compiler enables C, C++ and SystemC programs to be directly targeted into Xilinx devices without the need to manually create RTL. Vivado HLS is widely reviewed to increase developer productivity, and is confirmed to support C++ classes, templates, functions and operator overloading. Vivado 2014.1 introduced support for automatically converting OpenCL kernels to IP for Xilinx devices. OpenCL kernels are programs that execute across various CPU, GPU and FPGA platforms. The Vivado Simulator is a component of the Vivado Design Suite. It is a compiled-language simulator that supports mixed-language, Tcl scripts, encrypted IP and enhanced verification. The Vivado IP Integrator allows engineers to quickly integrate and configure IP from the large Xilinx IP library. The Integrator is also tuned for MathWorks Simulink designs built with Xilinx's System Generator and Vivado High-Level Synthesis.The Vivado Tcl Store is a scripting system for developing add-ons to Vivado, and can be used to add and modify Vivado's capabilities. Tcl is the scripting language on which Vivado itself is based. All of Vivado's underlying functions can be invoked and controlled via Tcl scripts.



Quick Start

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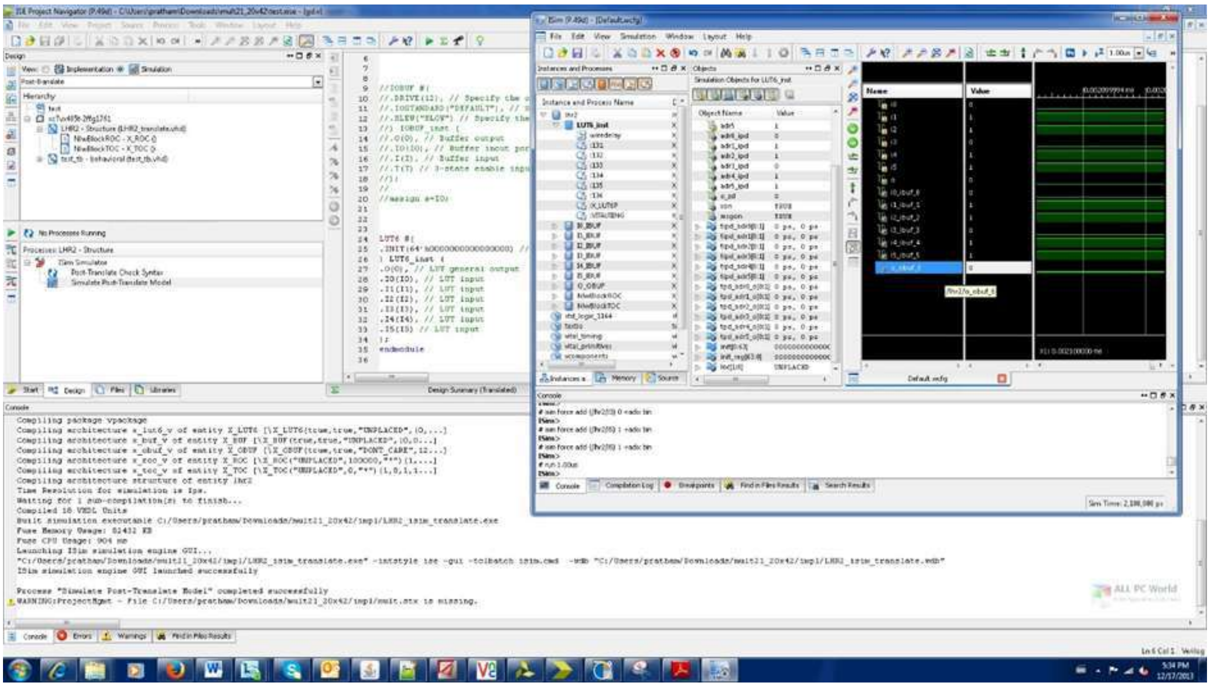
hw
/home/dan/code/github.com/mosscompute...



```
//IOBUF #(
//.DRIVE(12), // Specify the o
//.IOSTANDARD("DEFAULT"), // S
//.SLEW("SLOW") // Specify the
//) IOBUF_inst (
//.O(O), // Buffer output
//.IO(IO), // Buffer inout por
//.I(I), // Buffer input
//.T(T) // 3-state enable inpu
//);
//
//assign a=IO;



LUT6 #(
.INIT(64'h0000000000000000) //
) LUT6_inst (
.O(O), // LUT general output
.I0(I0), // LUT input
.I1(I1), // LUT input
.I2(I2), // LUT input
.I3(I3), // LUT input
.I4(I4), // LUT input
.I5(I5) // LUT input
);
endmodule
```

```
# isim force add {/lhr2/I3} 0 -radix bin
ISim>
# isim force add {/lhr2/I5} 1 -radix bin
ISim>
# isim force add {/lhr2/I6} 1 -radix bin
ISim>
# run 1.00us
ISim>
```

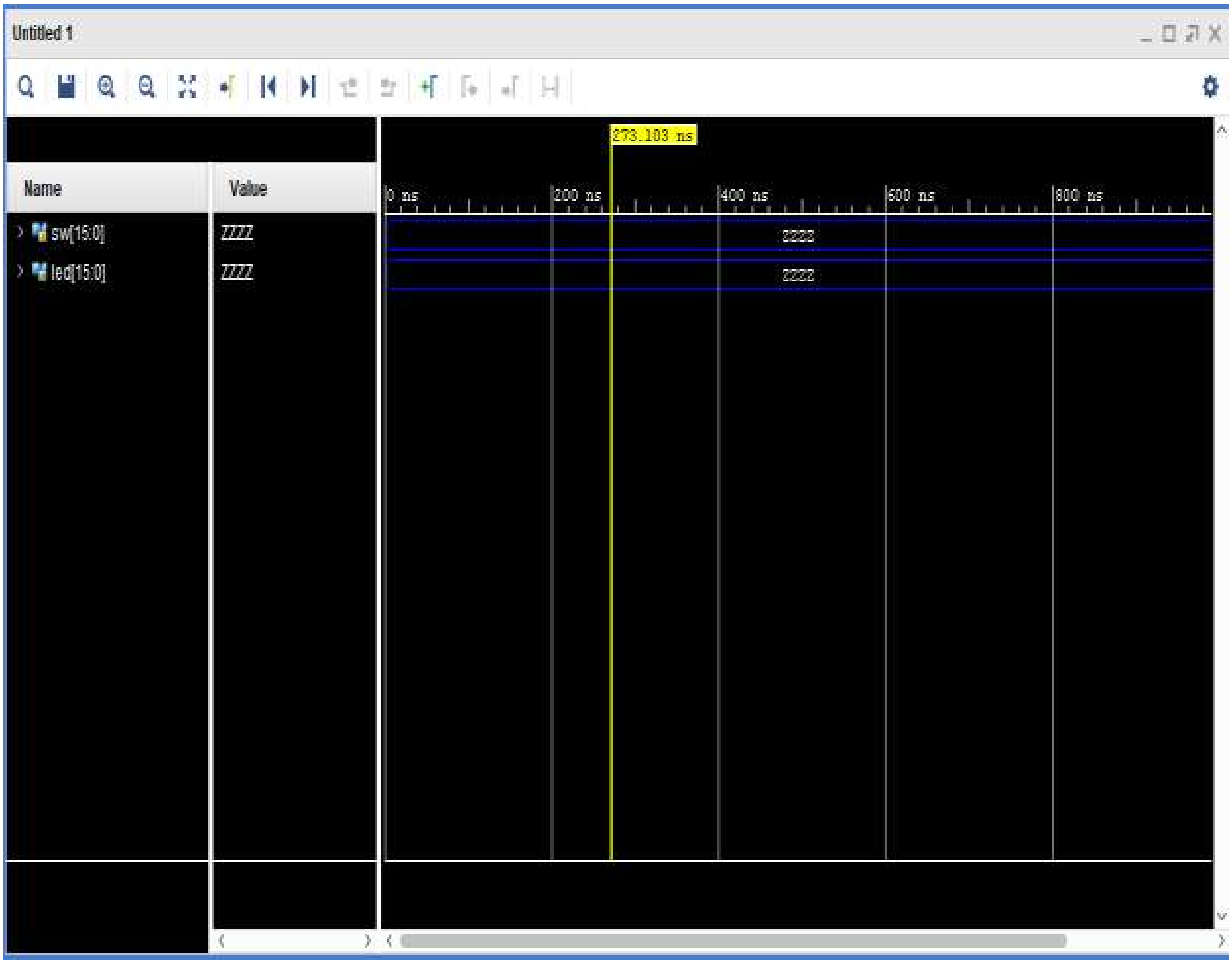
```
Compiling package vpackage
Compiling architecture x_lut6_v of entity X_LUT6 [\X_LUT6(true,true,"UNPLACED",(0,...]
Compiling architecture x_buf_v of entity X_BUF [\X_BUF(true,true,"UNPLACED",(0,0...]
Compiling architecture x_obuf_v of entity X_OBUF [\X_OBUF(true,true,"DONT_CARE",12...]
Compiling architecture x_roc_v of entity X_ROC [\X_ROC("UNPLACED",100000,"*")(1,...]
Compiling architecture x_toc_v of entity X_TOC [\X_TOC("UNPLACED",0,"*")(1,0,1,1...]
Compiling architecture structure of entity lhr2
Time Resolution for simulation is 1ps.
Waiting for 1 sub-compilation(s) to finish...
Compiled 18 VHDL Units
Built simulation executable C:/Users/pratham/Downloads/mult21_20x42/impl/LHR2_isim_translate.exe
Fuse Memory Usage: 82432 KB
Fuse CPU Usage: 904 ms
Launching ISim simulation engine GUI...
"C:/Users/pratham/Downloads/mult21_20x42/impl/LHR2_isim_translate.exe" -intstyle ise -gui -tclbatch isim.cmd  -wdb "C:/Users/pratham/Downloads/mult21_20x42/impl/LHR2_isim_translate.wdb"
ISim simulation engine GUI launched successfully

Process "Simulate Post-Translate Model" completed successfully
WARNING:ProjectMgmt - File C:/Users/pratham/Downloads/mult21_20x42/impl/mult.stx is missing.
```

SOURCE CODE

```
module sw_led(

// Slide switch inputs

input [15:0]sw,

// Led outputs

output [15:0]led

);

// Assign each sw to it's respective led

assign led[0] = sw[15];

endmodule
```

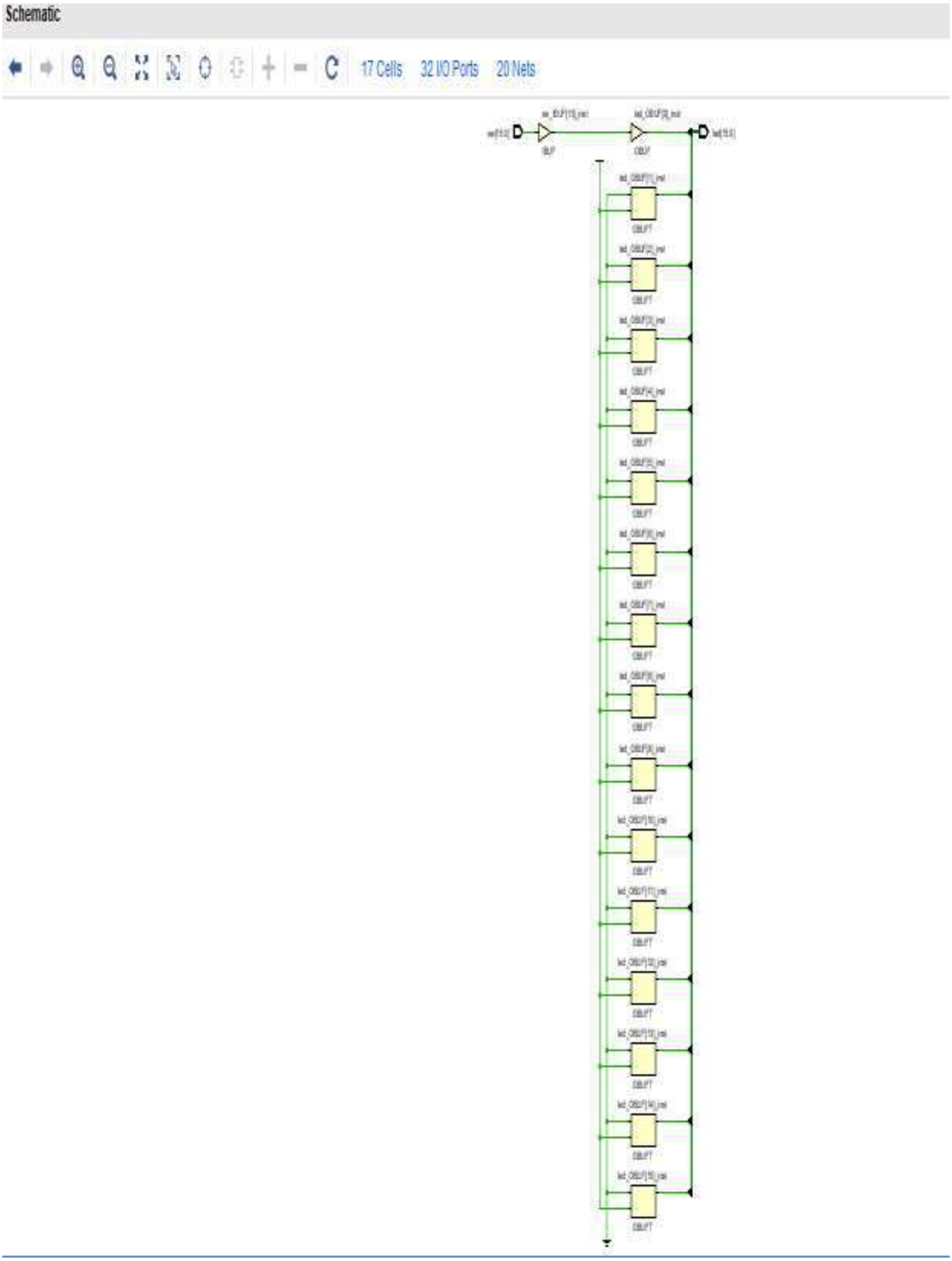
```
# Switches

set_property PACKAGE_PIN V17 [get_ports {sw[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]

set_property PACKAGE_PIN V16 [get_ports {sw[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]

set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]

set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]

set_property PACKAGE_PIN W15 [get_ports {sw[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[4]}]

set_property PACKAGE_PIN V15 [get_ports {sw[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[5]}]

set_property PACKAGE_PIN W14 [get_ports {sw[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[6]}]

set_property PACKAGE_PIN W13 [get_ports {sw[7]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[7]}]

set_property PACKAGE_PIN V2 [get_ports {sw[8]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[8]}]

set_property PACKAGE_PIN T3 [get_ports {sw[9]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[9]}]

set_property PACKAGE_PIN T2 [get_ports {sw[10]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[10]}]

set_property PACKAGE_PIN R3 [get_ports {sw[11]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[11]}]

set_property PACKAGE_PIN W2 [get_ports {sw[12]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[12]}]
set_property PACKAGE_PIN U1 [get_ports {sw[13]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[13]}]

set_property PACKAGE_PIN T1 [get_ports {sw[14]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[14]}]

set_property PACKAGE_PIN R2 [get_ports {sw[15]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[15]}]




# LEDs

set_property PACKAGE_PIN U16 [get_ports {led[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[0]}]

set_property PACKAGE_PIN E19 [get_ports {led[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[1]}]

set_property PACKAGE_PIN U19 [get_ports {led[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[2]}]

set_property PACKAGE_PIN V19 [get_ports {led[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[3]}]

set_property PACKAGE_PIN W18 [get_ports {led[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[4]}]

set_property PACKAGE_PIN U15 [get_ports {led[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[5]}]

set_property PACKAGE_PIN U14 [get_ports {led[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[6]}]

set_property PACKAGE_PIN V14 [get_ports {led[7]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[7]}]

set_property PACKAGE_PIN V13 [get_ports {led[8]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[8]}]

set_property PACKAGE_PIN V3 [get_ports {led[9]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[9]}]

set_property PACKAGE_PIN W3 [get_ports {led[10]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[10]}]
set_property PACKAGE_PIN U3 [get_ports {led[11]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[11]}]

set_property PACKAGE_PIN P3 [get_ports {led[12]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[12]}]

set_property PACKAGE_PIN N3 [get_ports {led[13]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[13]}]

set_property PACKAGE_PIN P1 [get_ports {led[14]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[14]}]

set_property PACKAGE_PIN L1 [get_ports {led[15]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {led[15]}]
```

SIMULATION

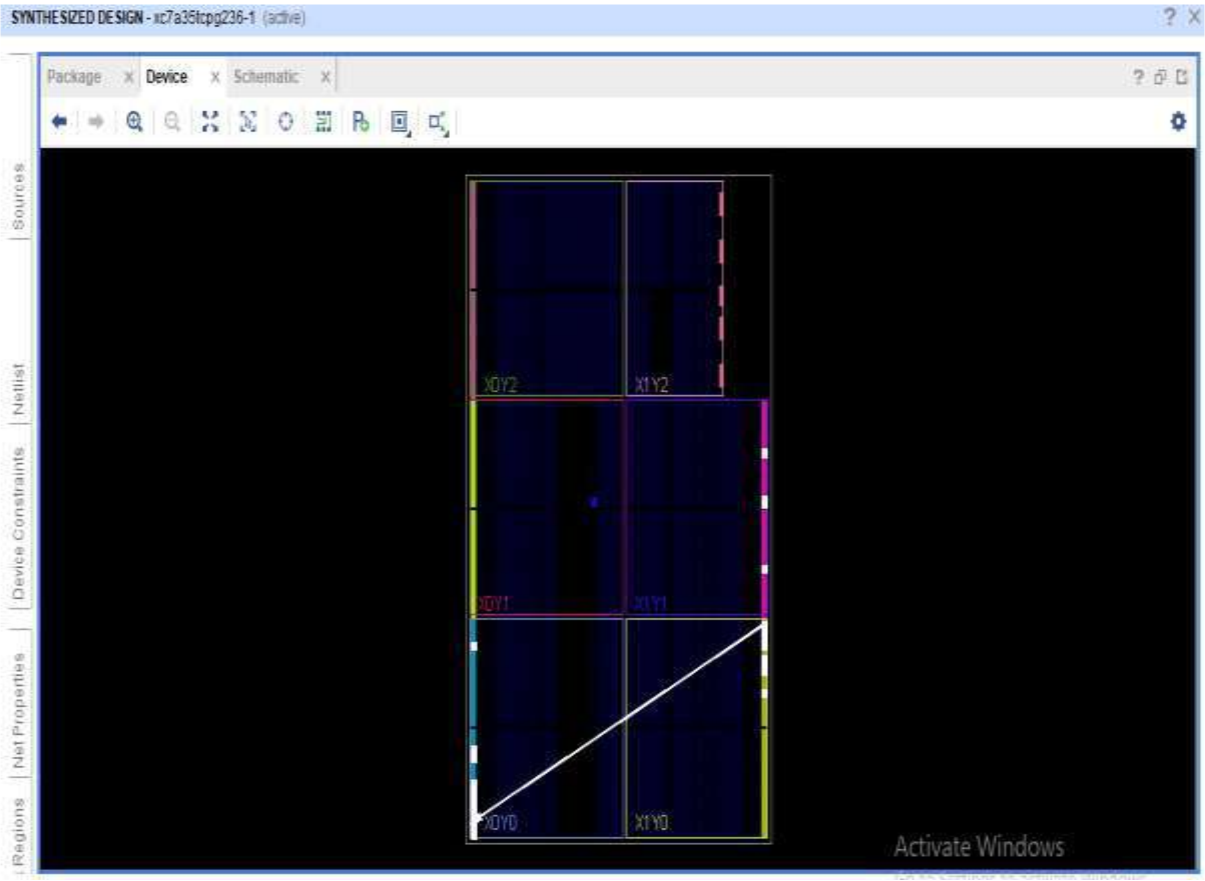


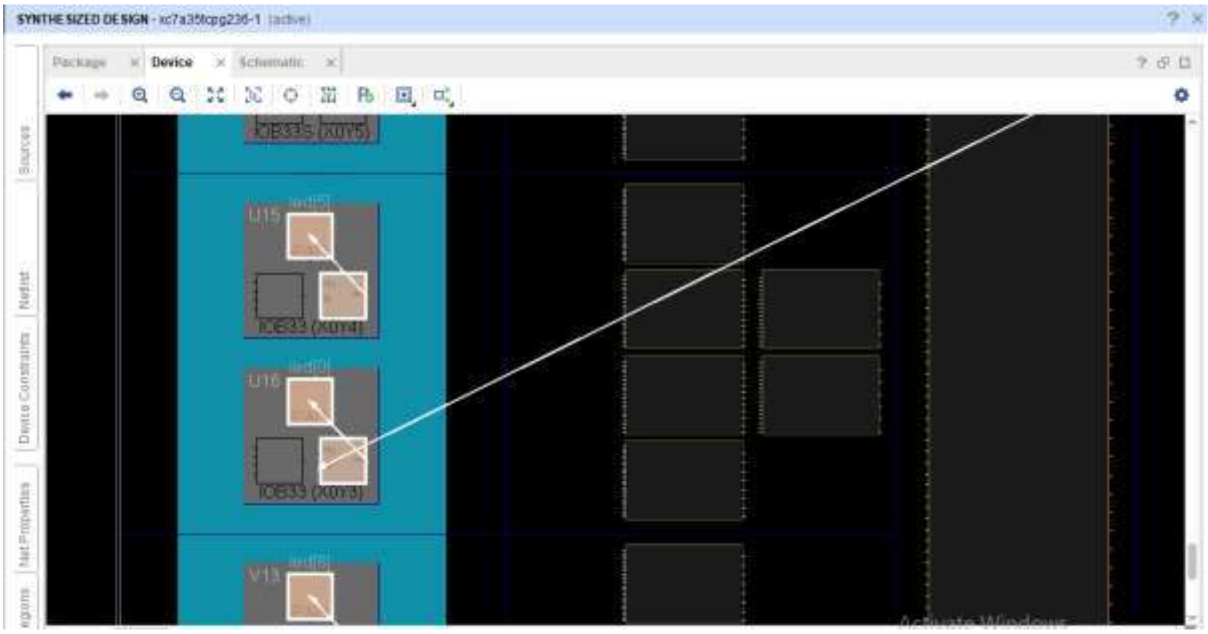
Name	Value
sw[15:0]	ZZZZ
led[15:0]	ZZZZ

SCHEMATIC


Schematic
17 Cells
32 I/O Ports
20 Nets
sw[15:0]
sw_IBUF[15]_inst
IBUF
led_OBUF[0]_inst
OBUF
led[15:0]
led_OBUF[1]_inst
OBUFT
led_OBUF[2]_inst
OBUFT
led_OBUF[3]_inst
OBUFT
led_OBUF[4]_inst
OBUFT
led_OBUF[5]_inst
OBUFT
led_OBUF[6]_inst
OBUFT
led_OBUF[7]_inst
OBUFT
led_OBUF[8]_inst
OBUFT
led_OBUF[9]_inst
OBUFT
led_OBUF[10]_inst
OBUFT
led_OBUF[11]_inst
OBUFT
led_OBUF[12]_inst
OBUFT
led_OBUF[13]_inst
OBUFT
led_OBUF[14]_inst
OBUFT
led_OBUF[15]_inst
OBUFT

DESIGN


SYNTHESIZED DESIGN - xc7a35tcpg236-1 (active)
Package
Device
Schematic
Sources
Netlist
Device Constraints
Net Properties
Regions
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Activate Windows


SYNTHESIZED DESIGN - xc7a35tcpg236-1 (active)
Package
Device
Schematic
Sources
Netlist
Device Constraints
Net Properties
Regions
IOB33S (X0Y5)
U15
led[5]
IOB33 (X0Y4)
U16
led[0]
IOB33 (X0Y3)
V13
led[6]
Activate Windows

CONLUSION

The workshop conducted at Rajagiri school of Engineering and Technology Kakkanad, Cochin helped to familiarize the basys 3 FPGA board, its usage and working. The classes conducted were online through AnyDesk platform. Students and Faculties participated in this workshop. They were divided into groups and each group was given a FPGA board. Thus understood the components of the board and simulation is done through vivado. The session was very informative and interesting.